Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a plurality of first bump electrodes arranged on a main surface, and each of said plurality of first bump electrodes receiving signals or power;

a plurality of dummy bump electrodes arranged on said main surface, and each of said plurality of dummy bump electrodes electrically connected to an associated one of said plurality of first bump electrodes wherein said plurality of dummy bump electrodes and said plurality of first bump electrodes being arranged alternately along to circumference of bump group.

2. (Previously Presented) The semiconductor device as claimed in claim 1 further comprising:

a plurality of protection circuits electrically coupled to said plurality of first bump electrodes.

3. (Original) The semiconductor device as claimed in claim 1, further comprising:

a plurality of test electrodes electrically connected to said first bump electrodes.

4. (Original) The semiconductor device as claimed in claim 3, wherein

said plurality of test electrodes being arranged along four edges of said semiconductor device.

5. (Previously Presented) The semiconductor device as claimed in claim 1, wherein said plurality of dummy bump electrodes being higher than a plurality of chip electrodes.

6. (Original) The semiconductor device as claimed in claim 1, wherein said plurality of dummy bump electrodes being arranged closer than said plurality of first bump electrodes.

7. (Previously Presented) The semiconductor device as claimed in claim 1, wherein said plurality of dummy bump electrodes being arranged between said plurality of first bump electrodes and a plurality of chip electrodes.

8. (Original) The semiconductor device as claimed in claim 1, wherein said plurality of dummy bump electrodes being provided for relaxation of stress at mounting said semiconductor device.

9.-11. (Cancelled)

12. (Previously Presented) A device comprising:

a substrate;

an insulating layer formed above said substrate;

a plurality of pads formed above said insulating layer;

a plurality of external bump electrodes formed above said insulating layer, and each electrically connected to an associated one of said plurality of pads; and

a dummy bump electrode formed above said insulating layer, and connected to associated one of said plurality of external bump electrodes.

13. (Previously Presented) The device as claimed in claim 12, wherein said dummy bump electrode being allocated between an associated one of said plurality of pads and an associated one of said plurality of external bump electrodes.

14. (Previously Presented) The device as claimed in claim 12, wherein said plurality of pads being allocated along an edge of said substrate.

15. (Previously Presented) The device as claimed in claim 13, wherein said plurality of pads being allocated along an edge of said substrate.

16. (Previously Presented) The device as claimed in claim 12, further comprising a first wiring connected between an associated one of said plurality of pads and an associated one of said plurality of external bump electrodes, and a second wiring connected between an associated one of said plurality of external bump electrodes and said dummy bump electrode.

17. (Previously Presented) The device as claimed in claim 12, wherein said plurality of pads are coupled to an internal circuit.

18. (Previously Presented) The device as claimed in claim 12, wherein said plurality of pads are coupled to a plurality of input/output buffers.

19. (New) A semiconductor device comprising:

a pad formed above a semiconductor chip;

a first bump electrode formed above said semiconductor chip corresponding to said pad;

a dummy electrode formed between said first bump electrode and said pad;

a first wiring connected between said first bump electrode and said pad; and

a second wiring connected between said dummy electrode or a portion near to said first bump electrode from a center of said first wiring and said pad.

20. (New) The semiconductor device as claimed in claim 19, wherein said dummy electrode is arranged in a first direction along a side of said chip.

21. (New) The semiconductor device as claimed in claim 19, wherein said first bump electrode is arranged internally from a side of said chip relative to said dummy electrode.